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Because the size of longs and pointers change in the LP64 data model, you need to be aware that this change alone can cause many **32-bit** to **64-bit** conversion ...

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Porting Device Drivers for the Solaris Operating System to **64-Bit** ...

Conversion from **32-bit** to **64-bit** code requires at minimum recompilation and re-linking with **64-bit** libraries. For cases in which **source code** changes are ...

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Solaris **64-bit** Developer's Guide

This chapter provides guidelines for writing code that works correctly in both **32-bit** and **64-bit** environments. At best, the **conversion** of current code might ...

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How to Automate Your **64-Bit** Migration—Part 1

In general, the migration of **32-bit source code** to **64-bit** will require the ... by the **conversion** of a portion of the application to **64-bit** execution. ...

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Oberon-2 from **32 bit** to **64 bit** – without any programming language ...

AOS is a set of several hundred Oberon-2 modules which compiles with A20 in either **32 bit** or **64 bit** mode without **source code** change. ...

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Developing **64-bit** Applications

ints are **32-bit**; longs are **64-bit**; long-longs are also **64-bit**; pointers are **64-bit**.

The use of the LP64 data model ensures that **source code** created for ...

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6502.org: **Source Code** Repository

The first is a **32-bit** multiply routine which computes a **64-bit** product and ...

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Programmer's Guide

All system interfaces use **64-bit** pointers. The **32-bit** pointer data type is ...

In general, the **conversion** of complex pointers requires **source code** changes. ...

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Time64 - **64-bit** version of C time routines for Windows

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(positions, colors, normals) may be specified by **32-bit** single precession IEEE floating point numbers, single precession IEEE floating point numbers, or **64-bit** double precision numbers. XGL, IrisGL, and OpenGL local modeling spaces are specified by full **32-bit** or **64-bit** floating-point coordinates. If sufficient
www.cse.ohio-state.edu/~hwshen/Su01_888/deering.pdf

[A Fast New DES Implementation in Software - Biham \(1997\) \(Correct\) \(37 citations\)](#)

bits, such as S boxes or eight-bit additions on **32-bit** processors) and when the word size of the than the fastest known DES implementation on a (**64-bit**) Alpha computer, and about three times faster for the encryption of each DES block. **Conversion** from and to the standard block representation
umjy.chonnam.ac.kr/~journey/cs/crypto/papers/cs0891.ps

[How to Use the Minimal Separators of a Graph for Its Chordal.. - Parra, Scheffler \(1994\) \(Correct\) \(21 citations\)](#)

[28] A. Parra and P. Scheer, How to use the minimal separators of a
ftp.math.tu-berlin.de/pub/Preprints/combi/Report-407-1994.ps.Z

[The Internet Streaming SIMD Extensions - Thakkar, Huff \(1999\) \(Correct\) \(17 citations\)](#)

involved the choice of either 2-wide or 4-wide **32bit** floating-point data parallel computations. This The basic approach was to double-cycle existing **64-bit** hardware. The performance benefit of selecting Passing parameters would either require more **conversion** instructions or would be through memory, as
developer.intel.com/technology/itj/q21999/articles/./pdf/simd_ext.pdf

[Challenges to Combining General-Purpose and Multimedia Processors - Conte, al. \(1997\) \(Correct\) \(14 citations\)](#)

in parallel on four 16-bit data types or on two **32-bit** data types (for more detail see the sidebar, the entire width of a processor data path (32 or **64 bits**) even when processing the small native data executions for arithmetic operations, data **conversion**, and rearrangement operations. Subword versions
www.ece.ncsu.edu/tinker/journal_papers/cm97.pdf

[A Data Parallel Finite Element Method for.. - Johan, Hughes.. \(1992\) \(Correct\) \(11 citations\)](#)

hardware, and up to 4 Mbytes of memory. There is a **32-bit** wide data path between each processing unit and node is composed of 32 one-bit processors and one **64-bit** floating-point accelerator, a routing chip and .11 4.2. Fortran 77 to Fortran 90 **conversion** .12 5.
www.cs.uh.edu/~johnsson/rpt/tr-02-92.ps.gz

[An Optimizer for Multimedia Instruction Sets - Cheong, Lam \(1997\) \(Correct\) \(11 citations\)](#)

point register file, sharing the **64-bit** and **32-bit** floating point registers. The Graphics Status the floating point register file, sharing the **64-bit** and **32-bit** floating point registers. The Graphics bytes or 16-bit words) within a wide (typically **64-bit**) data word on modern microprocessors. Other
www-suif.stanford.edu/suifconf/suifconf2/papers/21.ps

[Report on the AES Candidates - Baudron, Gilbert, Granboulan.. \(1999\) \(Correct\) \(6 citations\)](#)

be based on **64-bit** architectures rather than on **32-bit** ones. Microprocessor manufacturers are currently believe that future technologies will be based on **64-bit** architectures rather than on **32-bit** ones. most microprocessors already have some endianness **conversion** routines #BSWAP for Intel #which cost little
www.dmi.ens.fr/~baudron/aes1.pdf.gz

[Further Results and Considerations on Side Channel Attacks on RSA - Klima, Rosa \(2002\) \(Correct\) \(4 citations\)](#)

the information about Hamming weight of certain **32-bit** words produced in the process of decoding m by The padding consists of bit 1, 71 zero bits and a **64-bit** representation of the message bit length. The section 3 we present a very simple but efficient **conversion** of the Manger/Bleichenbacher breaking oracle to
eprint.iacr.org/2002/071.pdf

Design of a Flexible Open Platform for High.. - Choi, Decasper.. (1999) (Correct) (4 citations)
a PCI bus interface that can be operated in either **32 bit** or **64 bit** mode (the PE board uses it in **32 bit** line cards. Such cards can use either a 16 bit or **32 bit** Utopia interface, although some (including interface that can be operated in either **32 bit** or **64 bit** mode (the PE board uses it in **32 bit** mode)The www.tik.ee.ethz.ch/~keller/allerton99.ps

Multimedia Signal Processors: An Architectural Platform with.. - Chen, Kung (1998) (Correct) (3 citations)
for the ALUs or functional units is less than **32 bits**. Some of the ALUs are the split-ALUs which can 2 (Alus) Bar(18 Gb/s) Nec Risc Core A Simd 32/ **64-Bit** Bus 16 2.0 600 [19] V830r/av(Coprocessor 64(etc. ffl Image &video processing: resolution **conversion**, image enhancement, image restoration, image www.geocities.com/ykchen913/publications/new-mp.pdf

Network Time Protocol (NTP) - Mills (1985) (Correct) (3 citations)
1 January 1900. The integer part is in the first **32 bits** and the fraction part in the last **32 bits**, as and Formats NTP timestamps are represented as a **64-bit** fixed-point number, in seconds relative to 0000 convenient multiple-precision arithmetic and **conversion** to Time Protocol representation (seconds)but www.tzi.de/~cabo/pdf/rfc958.txt.pdf

Time Stamp Counters Library - Measurements with Nano Seconds .. - Etsion, Feitelson (2000) (Correct) (1 citation)
that is supported by the Intel hardware is only **32 bits** in size. Some compilers support **64 bit** integral 2.1 Types The hardware's time stamp counter is a **64 bit** integral register. Currently, the biggest represent all **64 bit** integer values, and since **conversion** to and from it incur unnecessary overhead, we www.cs.huji.ac.il/~etsman/docs/tsclib.ps

Automatic Software Optimization of Block Ciphers using Bitslicing .. - Pornin (1999) (Correct) (1 citation)
to the early seventies, what could be done with **32 bits** was already quite clear nowadays, we still see register size expansion is slow: 4 bits in 1971, **64 bits** in 1998 1 The register and logical over a bunch of registers this implies some **conversion** stages that may be rather slow. This problem is www.dmi.ens.fr/~pornin/bitslice.ps

CRYPTON: A New 128-bit Block Cipher - Specification and Analysis - Lim (1998) (Correct) (1 citation)
up to 256 bits (with increment by a multiple of **32 bits**) by iterating a fully parallelizable round such as software implementations on 8-bit, 16-bit, **32-bit** and **64-bit** microprocessors and a dedicated implementations on 8-bit, 16-bit, **32-bit** and **64-bit** microprocessors and a dedicated hardware crypt.future.co.kr/~chlim/pub/cryptonv05.ps

Low-Cost Double-Size Modular Exponentiation - Or How To (Correct)
common implementations take advantage of the 8 or **32-bit** host CPU to externally execute the work 2 we most e#orts focused on conventional 8, 16, 32 or **64-bit** architectures (we refer the reader to [7, 1, 2] Radix/Modular and Modular/Radix representation **conversions**. The next section sheds light on these www.gemplus.com/smart/rd/publications/ps/Pai99low.ps

Table Lookup Structures for Multiplicative Inverses Modulo 2 - David Matula Alex (Correct)
employing Equation 1 would be needed to obtain a **32-bit** integer modular inverse. Just two iterations for providing a seed inverse for obtaining 32/**64-bit** multiplicative inverses by one/two iterations of essentially a "discrete log triple transform"**Conversion** between standard binary and Benschop's exponent enr.smu.edu/~mitch/pubs/./ftp_dir/pubs/arith05.pdf

Ecma/tc39tg3/2000/3 - Draft Standard Ecma-Xxx (Correct)
yield short integer values actually leave an l4 (**32bit**) value on the stack, but it is guaranteed that arithmetic is available and efficient on current **64 bit** hardware. For this reason, numeric instructions significant bits are all zero for the unsigned **conversions** or a sign extension for the signed www.cs.ucsb.edu/~ckrintz/papers/Part_3_IL_Inst_Set.pdf.gz

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